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Hybrid Integrated Frequency Doublers and Triplers to 300 and 450 GHz

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Abstract—**High-power wide-band submillimeter-wave frequency sources have been developed. A frequency doubler to 300 GHz has delivered an output power of 5 mW with 3-dB-down bandwidth of more than 10 GHz. A frequency tripler to 450 GHz with an output power of 0.5 mW has also been tested. These multiplier output powers are highest values in the respective frequency regions up to date.**

The successful performances have been achieved by use of GaAs Schottky-barrier diodes and hybrid integrated circuits which are specially designed to obtain high output power.

I. Introduction

In recent years, the submillimeter-wave region has been investigated in the fields of radio astronomy, plasma diagnostics, spectroscopy, and Josephson detector research [1].

The authors and others have succeeded in obtaining frequency sources operating at up to 600 GHz by using frequency multipliers with GaAs Schottky-barrier diodes [2]. At 300 GHz, the obtained power was 0.7 mW by the hybrid integrated doubler [3] and 2 mW by the double ridged type tripler [4]. At 450 GHz, the output power was 0.12 mW by the hybrid integrated tripler [2]. However, these output power levels were too small compared with the power levels that were handled in the lower frequency regions for use in many applications and the output bandwidths were too narrow.

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In order to increase the output power of the submillimeter-wave multipliers, a special design, which is different from that in the millimeter wave region, is necessary. In the millimeter wave region, the multiplier performance primarily depends upon a diode figure of merit (diode cutoff frequency f_{cb}). The performance in the submillimeter wave region, however, is decided by an external circuit as well as f_{cb} due to the increased circuit loss and the difficulty of circuit impedance matching.

The authors designed and fabricated the multipliers, while paying attention to the above points, and obtained 5- and 0.5-mW output power readings in 300- and 450-GHz regions, respectively. In addition, the doubler to 300 GHz has shown wide-band characteristic with 3 dB-down width of more than 10 GHz.

This paper describes the diode and circuit designs, the fabrication techniques, the performances of the doubler to 300 GHz, and the measurement results for the tripler to 450 GHz.

II. Diode Design and Fabrication

A flow chart of the high-power multiplier fabrication sequence is shown in Fig. 1. The design and fabrication of the diode are described in the following, according to the flow chart.

A. Diode Fabrication

A principle of the frequency multiplier is harmonic generation by use of variable capacitance of the diode

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TABLE I
FABRICATED DIODES DC CHARACTERISTICS

Diode number	A	B	C	D	E	F	G	H	I	J	K
N_d (cm^{-3})	7.8×10^{16}	7.8×10^{16}	7.8×10^{16}	7.8×10^{16}	1.2×10^{17}	1.2×10^{17}	1.2×10^{17}	1.2×10^{17}	4.7×10^{17}	4.7×10^{17}	4.7×10^{17}
d (μm)	7.6	5.4	3.3	1.7	7.7	5.6	3.3	2.3	5.6	3.5	2.7
R_s (Ω)	7.0	8.0	14	48	5.5	5.7	9.8	13	5.5	5.4	6.3
V_b (volt) *	13.0	13.0	13.0	13.0	10.0	10.0	10.0	10.0	6.0	6.0	6.0
n	1.02	1.04	1.11	1.15	1.03	1.07	1.09	1.13	1.12	1.17	1.11

* values at 50 μA

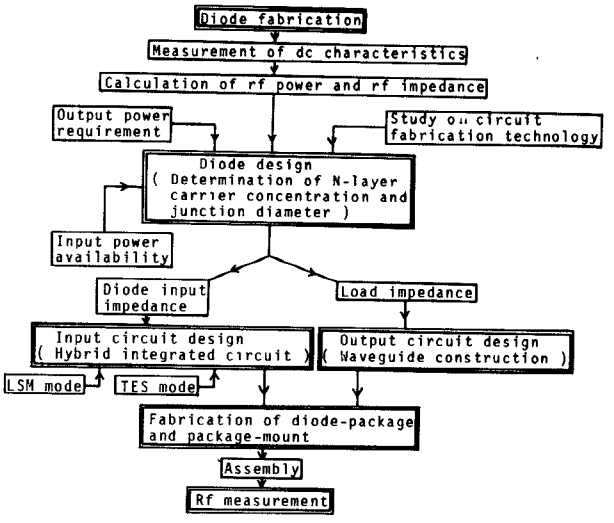

Fig. 1. Multiplier fabrication sequence flow chart.

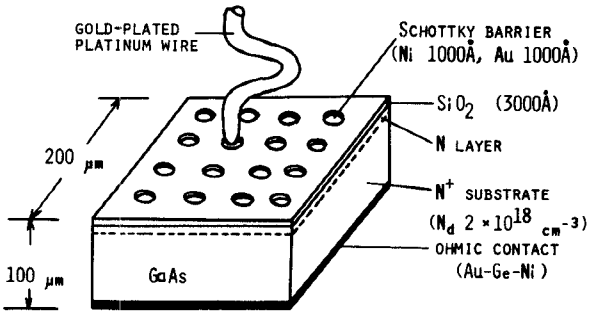

Fig. 2. GaAs Schottky-barrier diode structure.

junction. The multiplier performance depends upon diode cutoff frequency f_{cb} which is defined by the formula

$$f_{cb}=\frac{S_{\max}-S_{\min}}{2\pi R_s} \tag{1}$$

where $S_{\max}$ and $S_{\min}$ are maximum and minimum values of elastance and R_s is the series resistance of the diode [5]. If the diode is assumed to be fully pumped from contact potential ϕ to the breakdown voltage V_b, f_{cb} becomes

$$f_{cb}=\frac{1}{2\pi R_s C_{\min}} \tag{2}$$

where $C_{\min}$ is a junction capacitance at V_b, and represented as

$$C_{\min}=\frac{\pi d^2}{4}\sqrt{\frac{q\epsilon_s N_d}{2\{\phi-V_b-(kT/q)\}}} \tag{3}$$

in the case of abrupt junction, where d, q, ϵ_s, and kT/q are the junction diameter, electron charge, dielectric constant, contact potential, and thermal voltage, respectively. Important design parameters are carrier concentration of N layer N_d, thickness of N layer W, and junction diameter d.

In order to obtain the optimum diode parameters, diodes having different N_d and d values were fabricated (Table I). The structure of the GaAs Schottky-barrier honeycomb diode is shown in Fig. 2. The W for each diode was controlled to be the thickness of the depletion layer at V_b to take the unswept layer off. A detailed fabrication process of the diode is given elsewhere [2].

B. DC Characteristics

Before cutting the GaAs wafer into individual diode pellets, R_s, V_b, d, and ideality factor n were measured. The R_s, V_b, and n values were obtained from dc current–voltage characteristics measured by a curve tracer, and d was measured by a microscope. Measurement results are listed in Table I.

C. Doubler RF Power and RF Impedance Calculations

Penfield and Rafuse calculated input power P_{in}, output power P_{out}, input resistance R_{in}, and the load resistance R_L for doubler operation at maximum power output on the assumption that the varactor was the fully pumped abrupt junction [5]. Since the Schottky-barrier diode is an abrupt junction diode, Penfield's calculation results can be applied. Figs. 3–7 were calculated using the data in Table I. As the data in Table I are not the dc measurement values, the results of these figures have not taken into account an increase of R_s in RF condition due to skin effect. However, these results are useful as the first approximations which provide important design information. Fig. 3 shows f_{cb} versus d. The f_{cb} decreases as d increases and approaches d^{-2} asymptotic line. This is explained as follows.

The R_s of the diode, with the structure shown in Fig. 2, is represented by the equation

$$R_s=R_{\text{epi}}+R_{\text{sub}}+R_{\text{cont}} \tag{4}$$

where R_{epi}, R_{sub}, and R_{cont} are N-layer resistance, N^+ substrate resistance, and contact resistance between whisker and junction metal. The R_{sub} and the R_{cont} are nearly independent of the value of d. The R_{epi} is negligi-

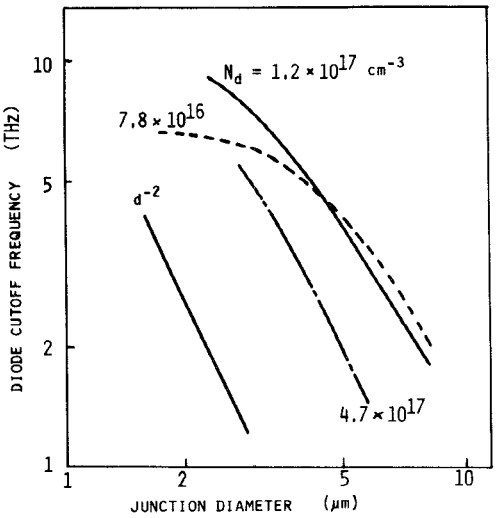

Fig. 3. Diode cutoff frequency versus junction diameter with N-layer carrier concentration as a parameter.

bly small compared with $R_{sub}+R_{cont}$ in the large d region. On the other hand, C_{min} increases in proportion to d^2. Therefore, f_{cb} is inversely proportional to d^2 in the large d region.

P_{in} and P_{out} as functions of d and N_d are shown in Figs. 4 and 5, respectively. If f_{cb} is much greater than the input frequency f_{in}, P_{out} is given by the formula [5]

$$P_{out}=0.0285(V_b+\phi)^2 2\pi f_{in}C_{min} \quad . \tag{5}$$

Accordingly, in order to obtain the large P_{out}, N_d should be made smaller and d large. However, P_{in}, which is required to obtain the P_{out}, also increases as N_d decreases and d increases, as shown in Fig. 4. For this reason, the input power availability limits the optimum values of d and N_d.

R_{in} and R_L also limit the optimum d and N_d. Figs. 6 and 7 show R_{in} and R_L as functions d and N_d, respectively. Since the characteristic impedance of the input circuit R'_{in} should be equal to R_{in} and the actually realizable values of R_{in} and R_L are finite, the maximum and minimum values of d and N_d are limited from the realizable range of R'_{in} and R_L.

D. Circuit Characteristic Impedance Limitation

As it is desirable to have large d to obtain large output power, R_{in} and R_L should be made small. A hybrid integrated circuit was proposed for the submillimeter wave multiplier, which could realize low characteristic impedance [2]. The hybrid integrated circuit is composed of microstriplines made by thin film on a quartz substrate. This kind of circuit was used for the high-power multiplier again.

There are two ways to make R_{in} small. The quartz substrate thickness should be made small and the stripline width should be made large. However, if the microstripline width is too large and approaches to the submillimeter wavelength, it becomes difficult to obtain the required characteristics [6]. The limit to the microstripline

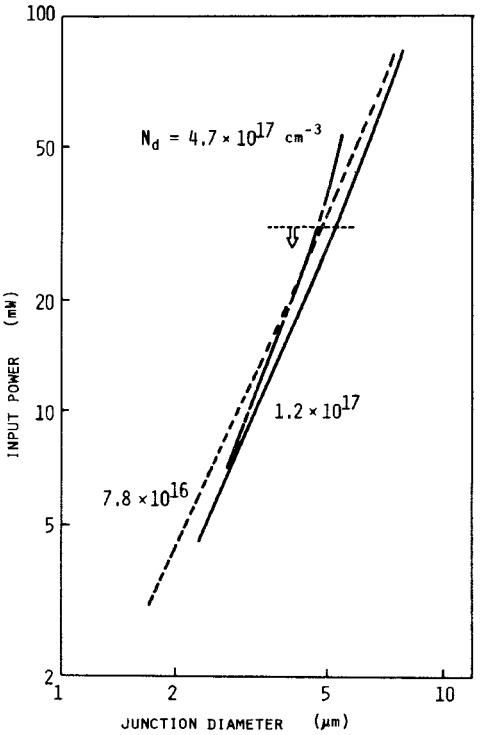

Fig. 4. Input power versus junction diameter with N-layer carrier concentration as a parameter. The broken line is the maximum input power delivered to the diode.

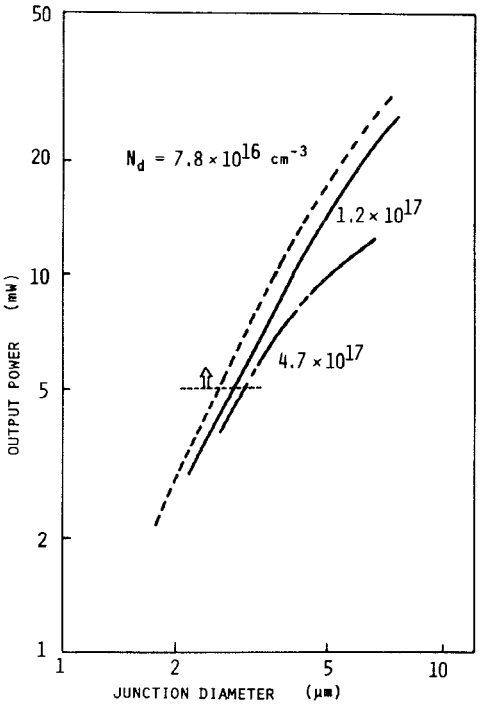

Fig. 5. Output power versus junction diameter with N-layer carrier concentration as a parameter. The broken line is the output power requirement value.

width is about 100 μm in the 300-GHz band. On the other hand, the quartz substrate can be thinned down to about 15 μm by today's polishing technology. Accordingly a 20-Ω minimum characteristic impedance can be realized for the multiplier input circuit.

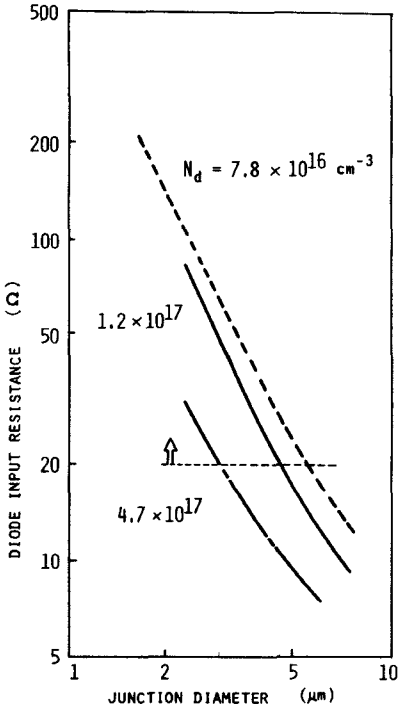

Fig. 6. Diode input resistance versus junction diameter with N-layer carrier concentration as a parameter. The broken line is the technologically possible minimum value of the input circuit impedance.

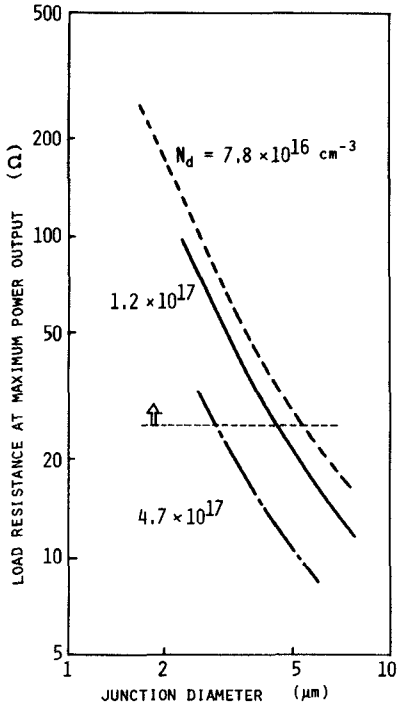

Fig. 7. Load resistance at maximum power output versus junction diameter with N-layer carrier concentration as a parameter. The broken line is the technologically possible minimum value of the output circuit impedance.

Since the hybrid integrated multiplier output circuit is a waveguide construction, it is necessary to reduce waveguide height to obtain low R_L. The 100-μm waveguide height has been fabricated by a groove cutting technique and 100-Ω characteristic impedance has been achieved. To realize a still lower R_L, a $\lambda_g/4$ line length impedance transformer can be used. In this way, 25-Ω characteristic impedance is obtained.

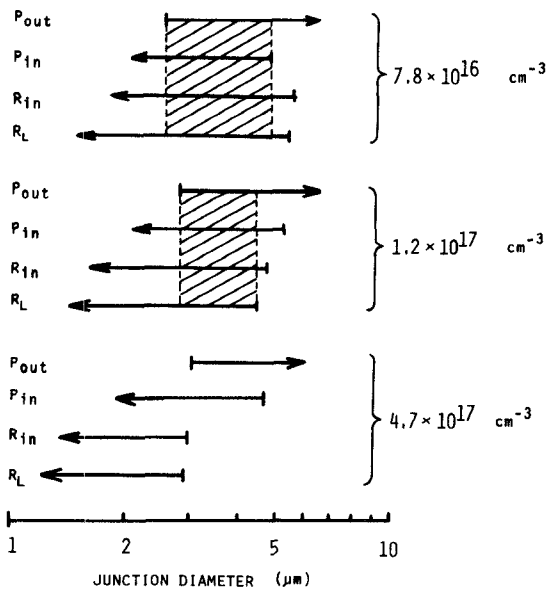

Fig. 8. Method of determining N-layer carrier concentration and junction diameter.

E. Input Power Limitation

Convenient oscillators in the 150-GHz band are IMPATT oscillators and klystrons to date. IMPATT oscillators generate 19-dBm power level in the 150-GHz band [7]. However, some problems remain to be solved because of difficulties in adjusting the frequencies. On the other hand, klystrons frequency adjustment is easy and they deliver about 18-dBm output power. Accordingly, a klystron was used as an input source for the multiplier. Taking the input circuit losses into account, it is inferred that the power delivered to the diode is about 15 dBm. This value was considered to be the limit of P_{in}.

F. Output Power Requirement

Considering using the multiplier as a local oscillator for 300-GHz band mixer or an input source for the frequency doubler to 600 GHz or tripler to 900 GHz, output power requirement value was planned to be more than 7 dBm.

G. N-Layer Carrier Concentration and Junction Diameter Determination

In summary, optimum N_d and d values to obtain P_{out} requirement value are determined from the following four parameter conditions: 1) required output power, 7 dBm; 2) maximum input power delivered to the diode, 15 dBm; 3) minimum input circuit impedance, 20 Ω; and 4) minimum load resistance, 25 Ω

Values for 1)–4) are indicated by broken lines in Figs. 4–7. From the cross points of these broken lines and the curves, the ranges of d to obtain the required P_{out} value are given. Fig. 8 shows these ranges of d for different N_d values. The hatched sections in Fig. 8 are the overlapped

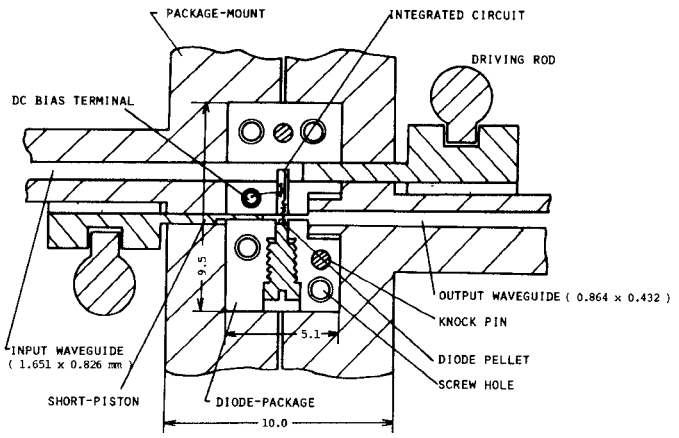

Fig. 9. Multiplier construction.

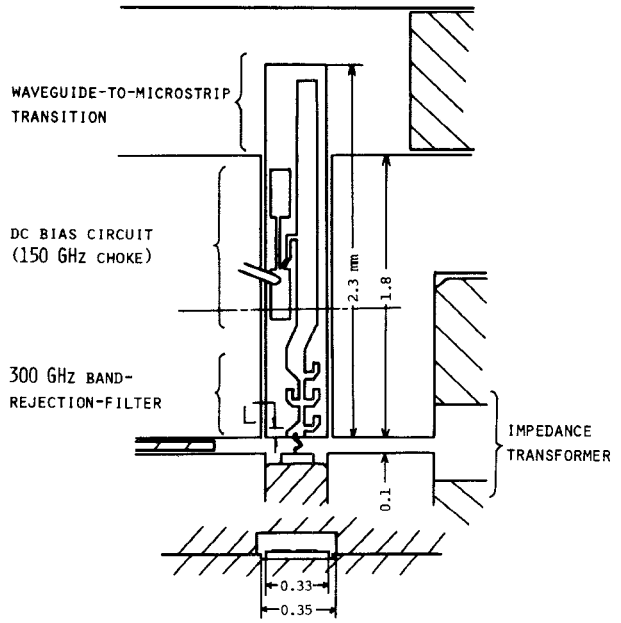

Fig. 10. Top and cross-sectional views of integrated circuit.

sections of these ranges. Using the diodes which have d and N_d in the overlapped sections, there is a possibility of attaining 7 dBm. A diode having 4.7×10^{17}-cm^{-3} N_d cannot realize the required output power, due to the lack of the overlapped section.

III. Circuit Design and Fabrication

Fig. 9 shows the construction of the doubler circuits which consists of a diode package and a package mount.

A. Input Circuit

Input circuits were integrated on a quartz substrate (0.33 mm wide, 2.3 mm long, and 15 μm thick), as shown in Fig. 10, mounted on the ground plane of the microstrip enclosure. The thin-film integrated circuit, which consisted of Cr (100-Å) and Au (1.5-μm) layers, was fabricated by evaporating, photolithography, and electroplating. Fabrication details for the thin-film circuit were

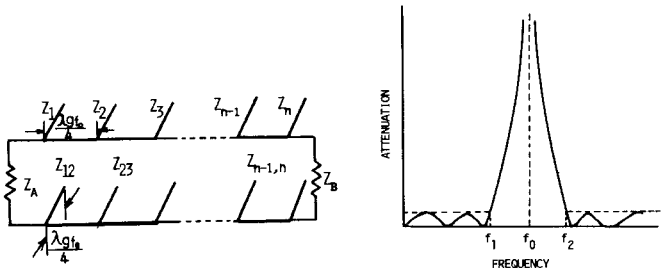

Fig. 11. n-stub transmission-line band rejection filter and its band rejection response.

reported previously [2]. The integrated circuit was composed of a waveguide (WR-6)-to-microstrip transition, a dc bias circuit (150-GHz choke), and a 300-GHz band rejection filter. For the design of these circuits, R_{in} must be determined first. If a diode having 1.2×10^{17}-cm^{-3} N_d and 3.5-μm d, which is located in the center of the common section in Fig. 8, is selected, R_{in} is determined to be 30 Ω from Fig. 6. However, since f_{cb} in RF condition is lower than that in dc condition due to the skin effect, R_{in} should be somewhat smaller than 30 Ω. For this reason, 20-Ω R_{in} was used in designing the circuits.

The waveguide-to-microstrip transition was made by a capacitance probe whose length was about a half of the waveguide height. The length was experimentally determined from a scaling experiment at 10-GHz band.

In order to reject the input wave propagation toward the dc bias port, 150-GHz RF choke was fabricated, which consisted of quarter-wavelength high-impedance lines and open-circuited low-impedance lines. Effective dielectric constant $\mathcal{K}_e$, for determining the length of each line, was obtained from Schneider's formula [8]

$$\mathcal{K}_e=\frac{\mathcal{K}+1}{2}+\frac{\mathcal{K}+1}{2}\left(1+\frac{10h}{W}\right)^{1/2} \tag{6}$$

where $\mathcal{K}$, h, and w are quartz dielectric constant (3.78), substrate thickness (15 μm), and microstrip linewidth (12 and 110 μm), respectively.

The dc bias terminal in the package was connected to a short-point of the low-impedance line with a 20-μm diameter wire by using an ultrasonic bonding technique. It was confirmed that the RF choke showed the wide-band characteristic, i.e., input wave propagation loss due to the existence of the bias circuit was measured and the loss was less than 0.6 dB over the 10-GHz bandwidth at the 151-GHz center frequency.

To prevent the propagation of second harmonics generated at the diode to the input port, a circuit which rejects a 300-GHz signal and transmits a 150-GHz signal is required. A Tchebyscheff-type band rejection filter, shown in Fig. 11 [9], was used for this purpose. The band rejection filter consists of $\lambda_g/4$ open-circuited stubs in series with $\lambda_g/4$ connected lines. The design was performed as follows. At first, a passband having Tchebyscheff ripple of 0.1 dB with the band edges at $f_1=170$

GHz and $f_2=430$ GHz was assumed. This settles the stopband center at the doubler output frequency

$$f_0=(f_1+f_2)/2=300\ \text{GHz}. \tag{7}$$

At least 30-dB attenuation at the frequency

$$f=f_0\pm 30\ \text{GHz}$$

was also assumed. Therefore, bandwidth parameter $\mathcal{Q}$ is

$$\mathcal{Q}=\cot(\pi/2\cdot f_1/f_0)=0.809. \tag{8}$$

A filter of this type has an attenuation characteristic related to that of a low-pass prototype filter. Then,

$$f'/f_1'=\mathcal{Q}\tan(\pi/2\cdot f_1/f_0)=5.11 \tag{9}$$

where f' and f_1' are frequency and cutoff frequency for the low-pass prototype filter. Therefore, the low-pass prototype should have at least 30-dB attenuation for $f'/f_1'=5.11$. In 0.1-dB ripple Tchebyscheff filter characteristic chart [9], it is found that the $n=3$ prototype has 37.5-dB attenuation. From a table of element values for Tchebyscheff filters, low-pass prototype parameters $g_0=1$, $g_1=1.1474$, $g_3=1.0315$, $g_4=1.000$, and $2\pi f_1'=1$ are given [9]. Since Z_A and Z_B correspond to R_{in}' and R_{in}, respectively, characteristic impedances for each line are calculated

$$\begin{aligned} Z_A&=Z_B=20\ \Omega\\ Z_1&=Z_3=44.0\ \Omega\\ Z_2&=21.6\ \Omega\\ Z_{12}&=Z_{23}=36.7\ \Omega. \end{aligned} \tag{10}$$

Since the characteristic impedance for each line was given, the linewidth was obtained [10] and then $\mathcal{K}_e$ was calculated from (6). Finally, the line length was obtained. $Z_2=21.6$-Ω stub was realized with two 43.2-Ω stubs in parallel, as shown in Fig. 10, so that narrower stubs have less junction effect.

A 150-μm-long 10-μm-diameter platinum whisker electroplated with 3000-Å thick gold was thermocompression bonded to an end of the circuit pattern.

A diode chip was soldered on top of the screw and was inserted into the lower side of the output waveguide and one of the honeycomb junction was connected to the whisker under a microscope.

B. Microstripline Higher Mode

Higher mode waves (Transvers-Electric-Surface mode) can propagate on the microstripline at frequencies higher than cutoff frequency f_{c1}. If TES mode waves exist on circuits designed by a dominant microstrip mode, pseudo-TEM mode, the circuits do not give the required characteristics. For this reason, f_{c1} must be higher than the doubler output frequency. The f_{c1} is given by the formula shown in [11]

$$f_{c1}=\frac{C_0}{4h\sqrt{\mathcal{K}-1}} \tag{11}$$

where C_0 is light velocity. Since f_{c1} becomes 3000 GHz for $h=15$ μm and $\mathcal{K}=3.78$, TES mode does not exist in the fabricated microstripline.

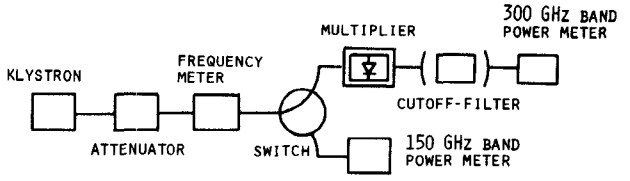

Fig. 12. Measurement setup.

C. Longitudinal Section Magnetic (LSM) Mode

It is also necessary to pay attention to generation of the quasi-rectangular waveguide mode, the LSM mode since the integrated circuit is shielded by a metal wall. Cutoff frequency f_{c2} for the LSM mode is represented by a formula shown in reference [12]

$$f_{c2}=\frac{C_0}{2A}\sqrt{1-\frac{h(\mathcal{K}-1)}{B\mathcal{K}}} \tag{12}$$

where A and B are width and height of the metal channel. f_{c2} should be made higher than the multiplier output frequency by making A small. B should be smaller than A for the same reason. However, if $B/h<5$, the calculation of the microstripline impedance becomes complicated due to the effect of the upper side wall [13]. Therefore, a B where $5h<B<A$ is preferable. Accordingly, microstrip channel having 300 μm for A and 100 μm for B was fabricated (f_{c2} is 404 GHz).

D. Output Circuit

The output circuit was fabricated in a rectangular waveguide construction. With a procedure similar to the R_{in}' design, R_L was determined to be 25 Ω. This value was attained by using $3\lambda g/4$ line-length impedance transformer which consists of 100-μm height waveguide in the diode-package and 430-μm height waveguide in the package mount, as shown in Fig. 9.

The output waveguide in the diode package, as well as the input waveguide and the microstrip ground plane, was fabricated by shaving brass with a diamond bit. The circuit loss was minimized by achieving a mirror-like surface, whose roughness was less than 1000 Å [3].

IV. Measurement and Results

Measurement setup used in the experiment is shown in Fig. 12. A 150-GHz klystron made by OKI Ceramic Co. was used as an input source. The output power at 300 GHz was measured with a commercial thin-film thermocouple calibrated by a dry calorimeter.

A. Doubler to 300 GHz

The doubler to 300-GHz experiment was accomplished using the G diode whose f_{cb} was 6.0 THz listed in Table I. To make the imaginary part of the diode impedance, owing to the junction capacitance and the whisker induc-

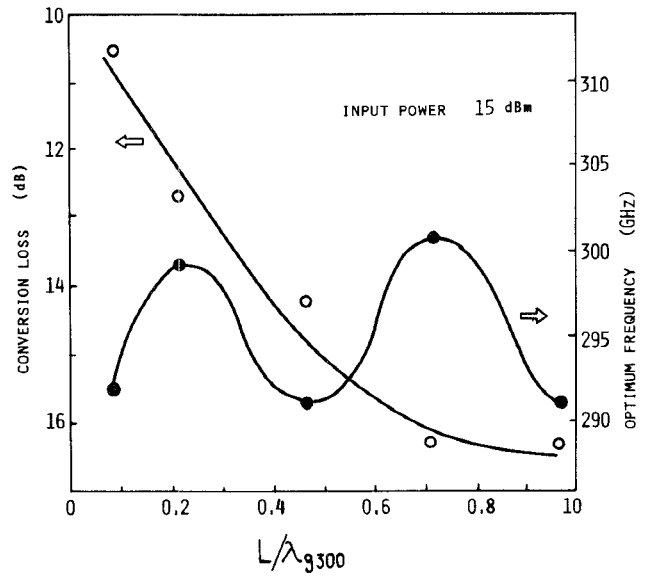

Fig. 13. Conversion loss and optimum frequency for 300-GHz doubler versus 300-GHz wavenumber of the distance from the filter edge to the upper side wall of the output waveguide.

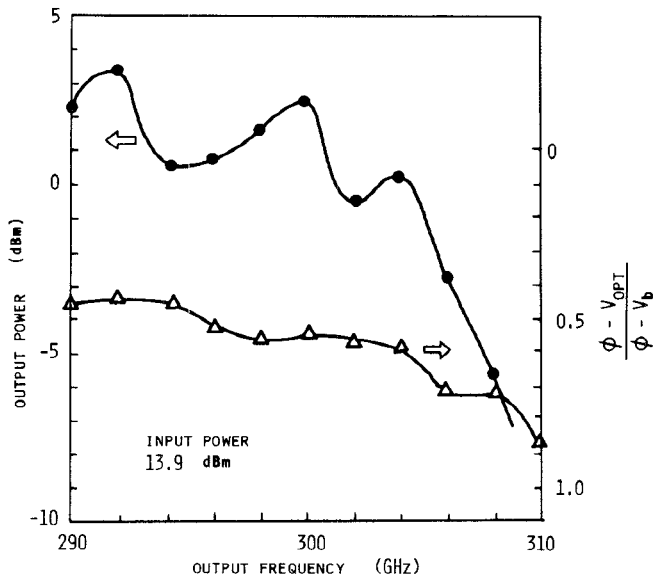

Fig. 14. Output power and optimum bias voltage V_{opt} for 300-GHz doubler as a function of output frequency.

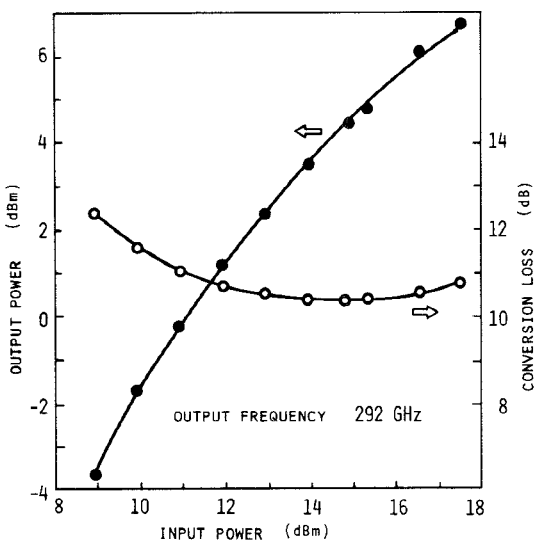

Fig. 15. Output power and conversion loss for 300-GHz doubler versus input power.

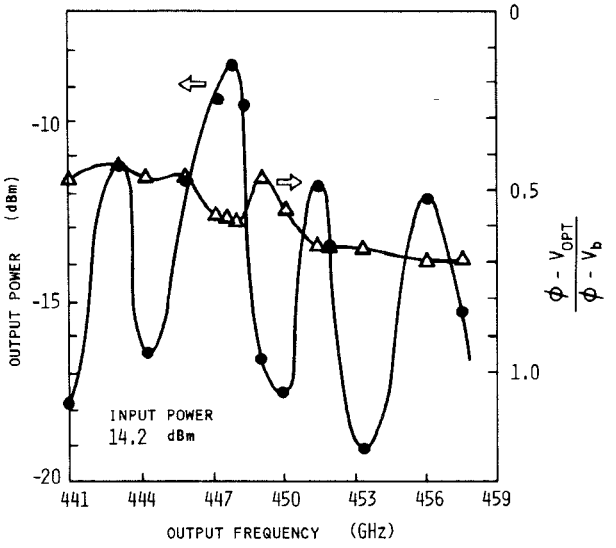

Fig. 16. Output power and optimum bias voltage V_{opt} for 450-GHz tripler as a function of output frequency.

tance, resonate at the output frequency by optimizing the length L shown in Fig. 10, five kinds of integrated circuits having different lengths L were tested. Measured conversion loss and an optimum frequency as a function of L/λ_{g300} are shown in Fig. 13. It is found that the optimum frequency varied periodically and the smallest L was preferable. The frequency characteristics for the output power and the optimum dc bias voltage V_{opt} are shown in Fig. 14. A 3-dB down bandwidth was more than 10 GHz. The optimum bias voltage approaches the breakdown voltage as frequency increases. This is explained as that the diode capacitance compensates for the increase in reactance due to frequency increase by varying bias voltage. Penfield *et al.* [5] reported that $(\phi - V_{opt})/(\phi - V_b)$ equals 0.35 for an operation at maximum power output. Since the value in the present experiment is 0.43 at the optimum frequency, it is found that the doubler circuits have been designed to be almost optimum.

Fig. 15 shows the output power versus input power relation. The 7-dBm maximum output power was achieved as projected in Section II-G. Minimum conversion loss was 10.3 dB.

B. Tripler Operation to 450 GHz

For multiplier tripler operation, a 350-GHz cutoff filter was connected after the output waveguide flange and different tuning was made from that for the doubler operation. The same diode and the same integrated circuit that was employed for the doubler were tested. The frequency characteristics of the output power and the optimum dc bias voltage V_{opt} are shown in Fig. 16. The

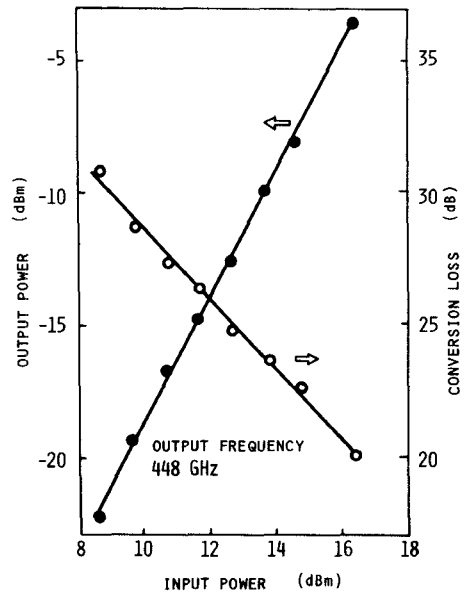

Fig. 17. Output power and conversion loss for 450-GHz tripler versus input power.

output power curve shows a fairly narrow-band characteristic as compared with the doubler. This resulted from the fact that the change in the idler condition with frequency change is considerable large, because of the large distance from the diode position and the short plane of the cutoff filter.

Fig. 17 shows output power and conversion loss versus input power for the tripler. The −3.5-dBm output power with 10.9-dB conversion loss exceeded the −9.3-dBm value reported in the previous paper [2]. Since the multiplier is designed as a doubler to 300 GHz and not studied in detail about idler circuits for the tripler, the larger output power and the wider bandwidth can be expected after the circuit design is completed.

V. Conclusion

High-power frequency doublers to 300 GHz have been developed and triplers to 450 GHz have also been tested.

The doubler design was accomplished by following procedure. Many kinds of diodes were fabricated first. Then, input and output powers and input and load resistances were calculated by using the dc measurement values for the fabricated diodes. Then, the diode design parameters were determined from the calculation results. Finally, multiplier circuits matched to the optimum diodes were designed and fabricated by means of a hybrid integrated circuit technique. As a result, a frequency doubler to 300 GHz and tripler to 450 GHz with output powers of 5 mW and 0.5 mW, respectively, which largely exceeded the previously obtained performances, have been developed. In addition, the doubler showed the wide-band characteristic such that 3-dB down bandwidth was more than 10 GHz.

This development of high-power wide-band frequency sources will result in many applications in the submillimeter wave region with advantages of being compact, being easy to handle, having wide-frequency tunability and long life.

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